REMARKS

Claims 1-2, 7, 9, 12-14, 27 and 37 are pending in the application.

Claims 1, 2 and 14 stand rejected under 35 U.S.C. §103(a) as unpatentable over U.S. Patent No. 6,506,642 to Luning et al., hereinafter, Luning, in view of U.S. Patent 6,258,680 to Fulford, Jr. et al, hereinafter, Fulford.

Claims 9 and 12 stand rejected under 35 U.S.C. §103(a) as unpatentable over Luning and Fulford, in view of U.S. Patent No. 6,730,556 to Wu et al., hereinafter, Wu.

Claims 13 and 37 stand rejected under 35 U.S.C. §103(a) as unpatentable over Luning and Fulford, in view of U.S. Patent No. 5,750,441 to Figura et al., hereinafter, Figura.

Applicants respectfully traverse the rejections based on the following discussion. The following paragraphs are numbered for ease of future reference.

I. The Prior Art Rejections

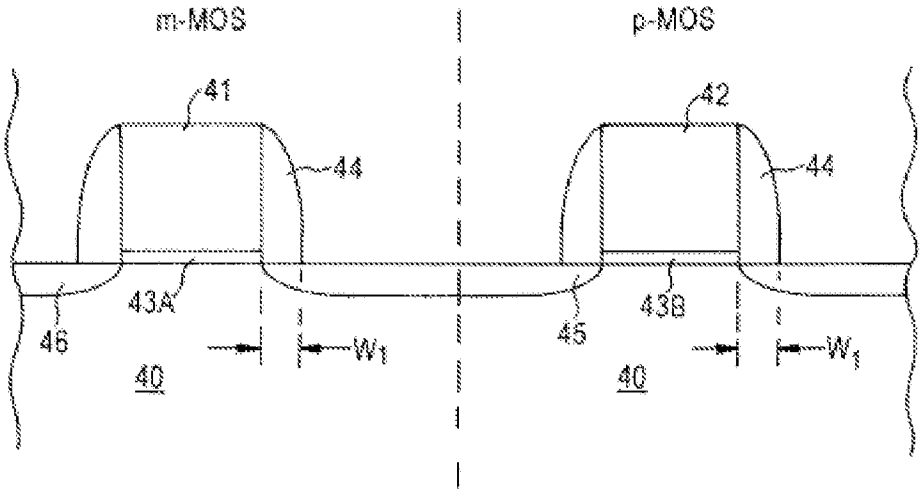
A. The 35 U.S.C. 103(a) Rejection over Luning and Fulford

1. The Luning Disclosure

[0001] It is a fact that Luning discloses, "Adverting to FIG. 4, first and second transistors, i.e. n-MOS and p-MOS transistors of a CMOS device, are formed, typically separated by a trench isolation containing a silicon oxide fill. First gate electrode 41 is formed over a semiconductor substrate 40 with first gate dielectric layer 43A therebetween in the n-MOS region, and second gate electrode 42 is formed over substrate 40 with second gate dielectric layer of 43B therebetween in the p-MOS region. Shallow source/drain extensions 45, 46 are then formed in a conventional manner employing gate electrodes 41 and 42 as masks. Subsequently, first sidewall spacer 44 is deposited on the side surfaces of the first and second gate electrodes 41, 42. Sidewall spacer 44 that has a width W_1 typically of about 600 to about 1,200 Å." (col. 4, lines 37-50).

[0002] It is a fact that FIG. 4 of Luning discloses,

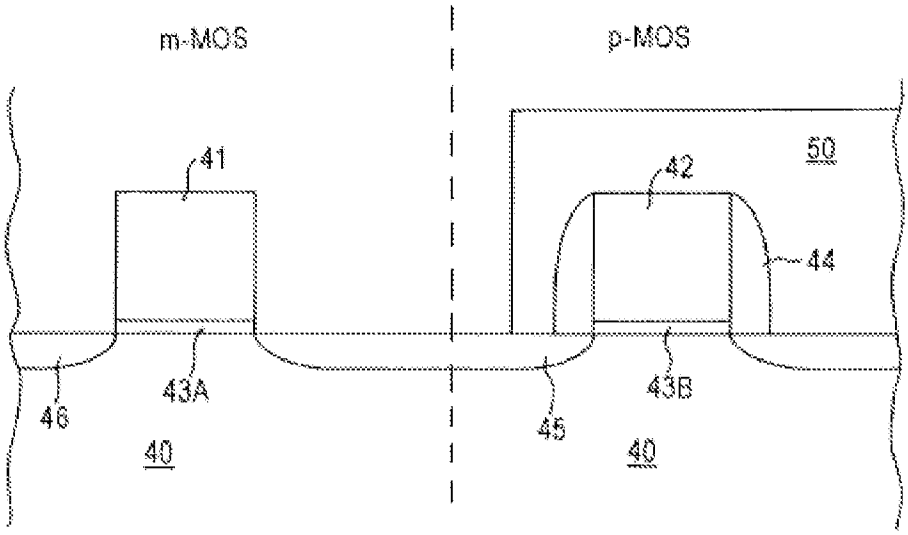
FIG. 4



[0003] It is a fact that Luning discloses, "Subsequently, as schematically illustrated in FIG. 5, a photoresist mask 50 is formed over the second gate electrode 42, inclusive of the first sidewall spacers 44, and etching is conducted to remove the first sidewall spacers 44 from the side surfaces of the first gate electrode 41, as by dry or plasma etching while adjusting etching conditions to achieve both vertical and lateral etching components thereby improving efficiency and reducing substrate damage. Subsequently, as illustrated in FIG. 6, second sidewall spacer 60 is then deposited on the side surfaces of the first gate electrode 41 and on the first sidewall spacers 44 positioned on the side surfaces of second gate electrode 42. Second sidewall spacer 60 is deposited at a width W_2 typically about 300 Å to about 900 Å. It can be appreciated from FIG. 6 that the width of the second sidewall spacer W_2 selectively controls the length of the source/drain extension 46 of the n-MOS transistor, while the thickness of the first and second sidewall spacers W_3, typically about 900 Å to 1,500 Å, controls the length of the source/drain extension of p-MOS transistor. Further, the thickness of the second sidewall spacer W_2 controls the distance between the metal silicide layer 64 and side surfaces of gate electrode 41, while the combined thicknesses W_3 of the first and second sidewall spacers separate the side surfaces of gate electrode 42 from metal silicide layer 63. (col. 4, line 51 to col. 5, line 8).

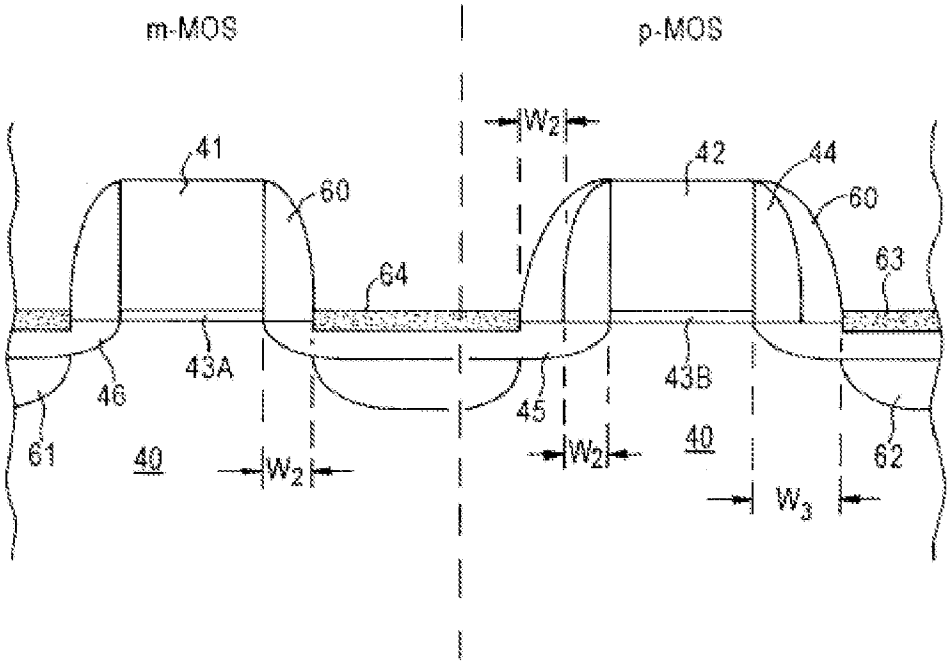
[0004] It is a fact that FIG. 5 of Luning discloses,

FIG. 5



[0005] It is a fact that FIG. 6 of Luning discloses,

FIG. 6



2. The Fulford Disclosure

[0006] It is a fact that Fulford discloses, "FIG. 11 illustrates another spacer formed from a conformal layer 158. Layer 158 is anisotropically etched, preferably using a plasma etch process, until layer 158 is cleared from the substantially horizontal planar regions of oxide layer 128 and oxide layer 146. By using an anisotropic etch and minimizing the overetch, spacer structures 160 and 162 are formed upon exterior sidewall surfaces of oxide spacers 148 and 150. The spacers are preferably nitride or polysilicon, which extend a horizontal distance d.sub.3 from opposing sidewall surfaces 116 and 120 of gate conductor 114, respectively." (col. 9, lines 4-14).

[0007] It is a fact that FIGs. 11 and 12 of Fulford disclose,

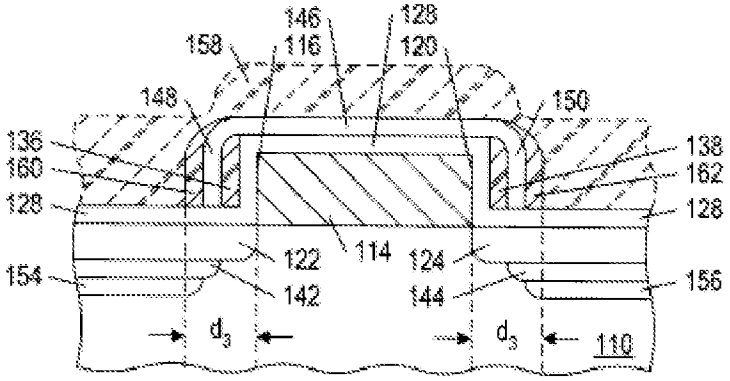


FIG. 11

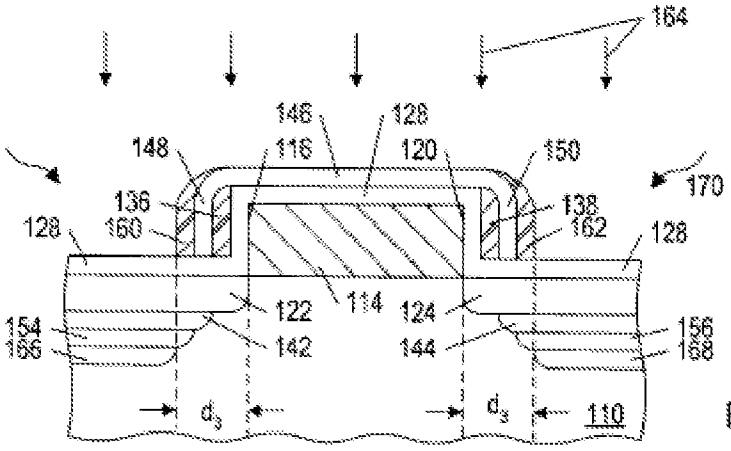


FIG. 12

3. Argument

[0008] The Office Action admits that "Luning does not specify an etch stop layer interposed between inner sidewalls of said second nitride spacers and said outer sidewall spacers of said first nitride spacers. Instead Luning recites merely that removal of the nitride sidewall spacers is effected by etching (col 4 ln 5-7)." (Office Action, mailed 12/24/2008, page 3, section 5).

[0009] The Office Action then asserts that "Fulford teaches in FIG 12 that an oxide etch stop layer (150) is interposed between a nitride spacer (138) and another nitride layer (158) to act as an etch stop so that a second set of nitride spacers can be formed (col 9 ln 4-12). It would have been obvious to one of ordinary skill in the art at the time the invention to use the teachings of Fulford in order to form a second set of nitride spacers." (Office Action, mailed 12/24/2008, page 3, section 6).

[0010] Applicants respectfully submit that the Office Action has misconstrued the functions of oxide layer 128, which acts as an etch stop, and oxide layer 150, which acts as a spacer, as argued fully below. (Please see, FIGs. 11 and 12 of Fulford, above).

[0011] It is a fact that Fulford discloses, "Oxide layer 128 is grown upon semiconductor substrate 110, upon upper surface 118 of gate conductor 114, and upon sidewall surfaces 116 and 120 of gate conductor 114 by oxidizing the silicon in those areas. Oxide layer 128 is to act as an etch stop during subsequent formation and removal of a spacer material set forth below." (col. 13-19). (emphasis added).

[0012] It is a fact that Fulford discloses, "FIG. 9 depicts an oxide layer 146 deposited upon the semiconductor topography. Oxide layer 128 is preferably deposited using a CVD process. If desired, an anisotropic etch may be used to remove the oxide from substantially horizontal surfaces. Resulting from deposition and possible etch, oxide layer 146 is formed above gate conductor 114 and immediately adjacent spacers 136 and 138 as oxide spacers 148 and 150. Oxide spacers extend a horizontal distance d_2 from sidewall surfaces 116 and 120 respectively. Distance d_2 is greater than distance d_1." (col. 8, lines 49-58).

[0013] As is known to those of ordinary skill in the art, an oxide layer may act, for example, as, an etch stop, a dielectric, a spacer, etc. Hence, an oxide layer is typically described

functionally, and one does not assume that, for example, an oxide layer described as a spacer also acts as an etch stop.

[0014] Fulford clearly describes his oxide layer 128 as an etch stop (col. 13-19), while describing oxide layer 150, resulting from the possible etch of progenitor oxide layer 146, as an oxide spacer (col. 8, lines 49-58).

[0015] Therefore, Applicants respectfully submit that the assertion by the Office Action, i.e., "Fulford teaches in FIG 12 that an oxide etch stop layer (150) is interposed between a nitride spacer (138) and another nitride layer (158) to act as an etch stop so that a second set of nitride spacers can be formed (col 9 ln 4-12). It would have been obvious to one of ordinary skill in the art at the time the invention to use the teachings of Fulford in order to form a second set of nitride spacers", (Office Action, mailed 12/24/2008, page 3, section 6), is incorrect.

[0016] For at least the reasons outlined above, Applicants respectfully submit that Luning and Fulford, either individually or in combination, do not disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", as recited in previously presented, independent claim 1. Accordingly, Luning and Fulford, either individually or in combination, fail to render obvious the subject matter of previously presented, independent claim 1 and dependent claims 2 and 14 under 35 U.S.C. §103(a). Withdrawal of the rejection of claims 1, 2, and 14 under 35 U.S.C. §103(a) as unpatentable over Luning and Fulford is respectfully solicited.

B. The 35 U.S.C. 103(a) Rejection over Luning, Fulford, and Wu

1. The Wu Disclosure

[0017] It is a fact that Wu discloses, "For example, assume in a first instance that area 16 is masked, and then an n-type dopant, such as arsenic, is implanted in area 14. This n-type implant forms HDD regions 26 that self-align with respect to sidewall spacers 25. Next, in a second instance, area 14 is masked, and then a p-type dopant is implanted in area 16. In the prior art, one common p-type dopant has been boron, and more recently favor has been found in the use of BF_2 rather than boron alone. This p-type implant forms HDD 46 regions that self-align

with respect to sidewall spacers 45." (col. 1, line 62 to col. 2, line 5).

2. Argument

[0018] The Office Action admits that "Luning and Fulford do not specify wherein a first impurity of said first impurity source/drain implant regions comprises arsenic, or wherein a second impurity of said second impurity source/drain regions comprises boron. Instead Luning discloses that the first impurity is n-type and that the second impurity is p-type." (Office Action, mailed 12/24/2008, page 4, section 12).

[0019] The Office Action then asserts, "Wu teaches that a suitable n-type dopant for CMOS transistors is arsenic, and a suitable p-type dopant for transistors is boron (col 1 ln 64—col 2 ln 2).

[0020] Applicants respectfully submit that nowhere does Wu disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", as recited in previously presented, independent claim 1.

[0021] Instead, Wu merely discloses that an n-type dopant may be arsenic (col. 1, line 64) and a p-type dopant may be boron (col. 2, line 2).

[0022] Wu does not cure the deficiencies of Luning and Fulford argued above.

[0023] For at least the reasons outlined above, Applicants respectfully submit that nowhere does Luning, Fulford and Wu, either individually or in combination, disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", as recited in previously presented, independent claim 1. Accordingly, Luning, Fulford and Wu, either individually or in combination, fail to render obvious the subject matter of previously presented, independent claim 1 and dependent claims 9 and 12 under 35 U.S.C. §103(a). Withdrawal of the rejection of claims 9 and 12 under 35 U.S.C. §103(a) as unpatentable over Luning, Fulford and Wu is respectfully solicited.

C. The 35 U.S.C. 103(a) Rejection over Luning, Fulford, and Figura

1. The Figura Disclosure

[0024] It is a fact that Figura discloses, "The second mask layer is a layer which can withstand an etch of the first mask (i.e. an etch stop layer) such as a low temperature chemical vapor deposited (CVD) oxide or nitride layer although other materials are possible." (col. 2, lines 52-56).

2. Argument

[0025] The Office Action admits that "Luning and Fulford disclose the CMOS device structure of claim 1, but do not specify wherein said etch stop layer comprises a low temperature oxide." (Office Action, mailed 12/24/2008, page 5, section 15).

[0026] Then Office Action then asserts, "Figura teaches that an etch stop layer preferably comprises a low temperature oxide so that the formation temperature is low enough to not disturb the previously formed layers (col 2 ln 57). It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Figura on the device of Luning and Fulford so as not to disturb the previously formed layer." (Office Action, mailed 12/24/2008, page 5, section 16).

[0027] Applicants respectfully submit that claim 37 recites in relevant part, "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", which is identical to the claim limitation argued above with respect to the rejection of claims 1, 2, and 14 under 35 U.S.C. §103(a) over Luning and Fulford. Therefore, Applicants respectfully invoke arguments identical to those argued above with respect to the rejection of claims 1, 2, and 14 over Luning and Fulford, for the rejection of previously presented, independent claim 37 over Luning, Fulford and Figura.

[0028] Figura does not cure the deficiencies of Luning and Fulford argued above.

[0029] Nowhere does Figura disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", as recited in previously presented, independent claims 1 and 37.

[0030] Instead, Figura merely disclose use of a low temperature oxide for an etch stop layer, where previous layers are deposited. (col. 2, lines 52-56).

[0031] For at least the reasons outlined above, Applicants respectfully submit that nowhere does Luning, Fulford and Figura, either individually or in combination, disclose, teach or suggest at least the present invention's features of: "an etch stop layer interposed between inner sidewalls of said second spacers and said outer sidewalls of said first spacers", as recited in previously presented, independent claims 1 and 37. Accordingly, Luning, Fulford and Wu, either individually or in combination, fail to render obvious the subject matter of previously presented, independent claim 37 and dependent claim 13, which depends from claim 1, under 35 U.S.C. §103(a). Withdrawal of the rejection of claims 13 and 37 under 35 U.S.C. §103(a) as unpatentable over Luning, Fulford and Figura is respectfully solicited.

II. Formal Matters and Conclusion

Claims 1-2, 7, 9, 12-14, 27 and 37 are pending in the application.

With respect to the rejections of the claims over the cited prior art, Applicants respectfully argue that the present claims are distinguishable over the prior art of record. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-2, 7, 9, 12-14, 27 and 37, all the claims presently pending in the application, are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest time possible.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

Dated: March 23, 2009

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